IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

re Application of: **Joel Hatsch et al.**	§	Group Art Unit: **2182**
Serial No.: **10/735,956**	§	Examiner:
Filing Date: **December 15, 2003**	§	Attny. Docket No. **068758.0151**
Title: **6-To-3 Bit Carry-Save Adder**	§	Client Ref.: **I0246US/lg/pp**

Mail Stop Missing Parts
Commissioner for Patents
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PURSUANT TO 37 C.F.R. § 1.10, I HEREBY CERTIFY THAT I HAVE INFORMATION AND A REASONABLE BASIS FOR BELIEF THAT THIS CORRESPONDENCE WILL BE DEPOSITED WITH THE U.S. POSTAL SERVICE AS EXPRESS MAIL POST OFFICE TO ADDRESSEE, ON THE DATE BELOW, AND IS ADDRESSED TO:

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INFORMATION DISCLOSURE STATEMENT

Sir:

Applicants respectfully request, pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, that the art listed on the attached PTO-1449 form be considered and cited in the examination of the above-identified application. A copy of the cited art is enclosed for the convenience of the Examiner.

Furthermore, pursuant to 37 C.F.R. §§1.97(g) and (h), no representation is made that these references are material to the patentability of the present application.

As the Information Disclosure Statement is being submitted before the mailing of the first office action on the merits, Applicants believe that no fee is required. If a fee is

required, please accept this transmittal as a petition therefor and charge any fee to Baker Botts L.L.P. *(formerly, Baker & Botts, L.L.P.)* Deposit Account No. 02-0383, Order No. (***068758.0151***) for any other charges necessary for the filing of this Information Disclosure Statement.

BAKER BOTTS L.L.P. (023640)

Date: April 5, 2004

By: _____

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(Limited recognition 37 C.F.R. §10.9)
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PTO-1449

Information Disclosure Citation in an Application

Application No.	Applicant(s):
10/735,956	Joel Hatsch et al.

Docket Number	Group Art Unit	Filing Date
068758.0151	2182	December 15, 2003

U.S. PATENT DOCUMENTS

		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	1	3,757,098	09-04-73	Wright	235	175	05-12-72
	2	5,504,915	04-02-96	Rarick	395	800	08-05-93
	3	6,345,286	02-05-02	Dhong et al.	708	708	10-30-98

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

NON-PATENT DOCUMENTS

		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)	DATE
	4	P.J. Song, et al.; "Circuit and Architecture Trade-Offs for High-Speed Multiplication; IEEE Journal of Solid-State Circuits; New York, US, Vol. 26, No. 9, pp. 1184-1198	09-01-91
	5	Zhongde Wang, et al.; "An Architecture for Parallel Multipliers"; IEEE Comp. Soc., Press, US, vol. 1, pp. 403-407	11-1991
	6	J.V. Salmon et al.; "Syntactic translation and logic synthesis in Gatemap"; IEEE Proceedings E. Computers & Digital Techniques; Institution of Electrical Engineers, Stevenage, GB; vol. 136; No. 4, part E, pp. 321-328	07-01-89
	7	Dinesh Somasekhar et al.; "Differential Current Switch Logic: A Low Power DCVS Logic Family"; IEEE Journal of Solid-State Circuits; IEEE Inc., New York, Vol. 31, No. 7, pp. 981-991	07-10-96

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.